

FORM PTO-1449 (REV.7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 98-P-009D1 (850063.529D1)		APPLICATION NO.	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANTS Shin Hwa Li et al.			
				FILING DATE December 22, 2003		GROUP ART UNIT	
U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
AC	AA	4,983,546	01/08/91	Hyun et al.	438	800	
	AB	5,169,491	12/08/92	Doan	156	636	
	AC	5,437,763	08/01/95	Huang	216	18	
	AD	5,468,682	11/21/95	Homma	438	633	
	AE	5,485,035	01/16/96	Lin et al.	257	637	
	AF	5,503,882	04/02/96	Dawson	427	579	
	AG	5,518,962	05/21/96	Murao	438	624	
	AH	5,560,802	10/01/96	Chisholm	156	636.1	
	AI	5,567,661	10/22/96	Nishio et al.	438	800	
	AJ	5,607,880	03/04/97	Suzuki et al.	438	624	
	AK	5,661,084	08/26/97	Kuo et al.	438	624	
	AL	5,747,381	05/05/98	Wu et al.	438	624	
	AM	5,783,482	07/21/98	Lee et al.	438	624	
	AN	5,858,882	01/12/99	Chang et al.	438	761	
	AO	6,001,731	12/14/99	Su et al.	438	633	
	AP	6,110,831	08/29/00	Cargo et al.	438	692	
	AQ	6,127,261	10/03/00	Ngo et al.	438	633	
AR	6,281,112	08/28/01	Sugiyama	438	624		
FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION			
				YES	NO		
AC	AS	0599317A1	06/01/94	EP			
	AT	09223740	08/26/97	Japan (Abstract only)			
	AU	08255791	10/01/96	Japan (Abstract only)			
EXAMINER <i>AC</i>				DATE CONSIDERED <i>7/15/04</i>			
* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).							

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	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	AK					
	AL					
	AM					
	AN					
	AO					

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AC	AV	Wolf, Stanley, PhD., Silicon Processing for the VLSI Era, Volume 2-Process Integration, Lattice Press, Sunset Beach, Volume 2: 334-337, 1990.
	AW	Schaffer, W.J., et al., "BPSG Improves CPMP Performance for Deep Submicron Ics," Semiconductor International, 205-212, 1996.
	AX	Armstrong, W.E., et al., "A Scanning Electron Microscope Investigation of Glass Flow in MOS Integrated Circuit Fabrication," Journal of the Electrochemical Society, Volume 121, No. 2, 307-310, 1974.
AC	AY	Kerr, D.R., et al., "Stabilization of SiO ₂ Passivation Layers with P ₂ O ₅ ," IBM Journal of Research and Development, Volume 8, No. 4, 376-384, 1964.

EXAMINER	DATE CONSIDERED
* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 409. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).	4/15/04